What is claimed is:

1. A designer configurable processor comprising:

a. a plurality of designer configurable computational units operating in parallel;

b. a memory device that communicates with the plurality of computational units through a data communication module; and

c. a software development tool that configures the plurality of computational units and a data path though the data communication module.

2. The processor of claim 1 wherein the designer configurable processor comprises a Very Long Instruction Word (VLIW) processor task engine.

3. The processor of claim 1 wherein the data communication module comprises a register routed data communication module.

4. The processor of claim 1 wherein the memory device stores at least one of data and instruction code.

5. The processor of claim 1 further comprising a task queue that communicates with the data communication module, the task queue scheduling tasks for the processor.

6. The processor of claim 5 wherein the task queue comprises a task queue controller module that communicates with the data communication module and a task queue module that communicates with task queue bus.

7. The processor of claim 6 further comprising an instruction memory that communicates with the task queue controller module, the instruction memory storing tasks for the processor.

8. The processor of claim 1 wherein the software development tool comprise at least one of a compiler, an assembler, an instruction set simulator, or a debugging environment.

9. The processor of claim 1 wherein the software development tool comprises a graphical interface that visually illustrates the configuration of the processor.

10. The processor of claim 1 wherein the software development tool generate a synthesizable RTL description of the processor.

11. The processor of claim 1 wherein the software development tool configures a data path from the processor to an input/output module.

12. The processor of claim 11 wherein the software development tool configures a width of the data path from the processor to the input/output module.

13. The processor of claim 1 wherein the software development tool configures a data routing path of at least one of the plurality of computational units.

14. The processor of claim 1 wherein the software development tool configures an instruction execution speed of at least one of the plurality of computational units.

15. The processor of claim 1 wherein the software development tool configures an energy required to operate at least one of the plurality of computational units.

16. The processor of claim 1 wherein the software development tool configures an instruction set of at least one of the plurality of computational units.

17. The multi-processor system of claim 1 wherein at least one of the plurality of designer configurable computational units comprises a set of input registers and a set of result registers.

18. A designer configurable multi-processor system comprising:

a. a plurality of designer configurable processors, each of the plurality of processors comprising a plurality of designer configurable computational units operating in parallel;

b. a memory device that communicates with the plurality of computational units through a data communication module;

c. an input/output (I/O) module that communicates with at least one of the plurality of processors through an I/O bus; and

d. a software development tool that configures the multi-processor system.

19. The multi-processor system of claim 18 wherein at least one of the plurality of plurality of processors comprises a Very Long Instruction Word (VLIW) processor.

20. The multi-processor system of claim 18 further comprising an instruction memory device that communicates with at least one of the plurality of processors.

21. The multi-processor system of claim 18 wherein the software development tool generates a synthesizable RTL description of at least one of the plurality of processors.

22. The multi-processor system of claim 18 wherein the software development tool configures a data path to the I/O module.

23. The multi-processor system of claim 22 wherein the software development tool configures a width of the data path to the I/O module.

24. The multi-processor system of claim 18 wherein the software development tool configures a data routing path of at least one of the plurality of computational units.

25. The multi-processor system of claim 18 wherein the software development tool configures an instruction execution speed of at least one of the plurality of computational units.

26. The multi-processor system of claim 18 wherein the software development tool configures an energy required to operate at least one of the plurality of computational units.

27. The processor of claim 18 wherein the software development tool configures an instruction set of at least one of the plurality of computational units.

28. A method of defining a computational unit for a multi-processor hardware system, the method comprising:

a. defining an architecture of at least computation unit in a Very Long Instruction Word (VLIW) processor with a software development tool; and

b. generating data from the software development tool that integrates the at least one computation unit into the VLIW processor task engine.

29. The method of claim 28 further comprising defining a data path width of the at least one computation unit with the software development tool.

30. The method of claim 28 further comprising defining an internal data routing path of the at least one computation unit with the software development tool.

31. The method of claim 28 further comprising defining an energy used to operate the at least one computation unit with the software development tool.

32. The method of claim 28 further comprising defining an instruction speed of the at least one computation unit with the software development tool.

33. The method of claim 28 further comprising defining an instruction set of the at least one computation unit with the software development tool.

34. The method of claim 28 further comprising performing a consistency check to validate the multi-processor hardware system.

35. The method of claim 28 wherein the generating data from the software development tool comprises generating scripts for an electronic design automation tool.